| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 29 | 187860 | ((transistor with (drain source channel)) with implantation implant$3) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:07 |
| 30 | 11490 | (((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:08 |
| 31 | 812 | ((((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2))) and (mobility mobilities) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:09 |
| 32 | 288 | (((((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2))) and (mobility mobilities)) and stress$3 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:11 |
| 33 | 157 | ((((((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2))) and (mobility mobilities)) and stress$3) and (compress$3 tensile) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:11 |
| 34 | 11088 | (((transistor with (drain source channel)) with implantation implant$3)) and ((implant$2 implantation implanting) with (void cavity cavities buble $5buble gas$2)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:07 |
| 35 | 19353 | transistor with (implantation implant$3) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:08 |
| 37 | 989 | (transistor with (implantation implant$3)) and (void cavity cavities buble $5buble ) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:09 |
| 38 | 416 | ((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble )) and (mobility mobilities carrier) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:10 |
| 39 | 399 | (((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble )) and (mobility mobilities carrier)) and source | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:10 |
| 40 | 356 | ((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble )) and (mobility mobilities carrier)) and source) and drain | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:10 |
| 41 | 351 | (((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble )) and (mobility mobilities carrier)) and source) and drain) and region | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:10 |

| | | | | |
|---|---|---|---|---|
| 42 | 316 | ((((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble )) and (mobility mobilities carrier)) and source) and drain) and region) and channel | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:11 |
| 43 | 130 | (((((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble )) and (mobility mobilities carrier)) and source) and drain) and region) and channel) and stress$3 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:11 |
| 44 | 45 | ((((((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble )) and (mobility mobilities carrier)) and source) and drain) and region) and channel) and stress$3) and (compress$3 tensile) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:23 |
| 45 | 1 | | USPAT | 2003/05/12 14:16 |
| 46 | 1 | | USPAT | 2003/05/12 14:16 |
| 47 | 610 | (transistor with (implantation implant$3)) and void | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:24 |
| 50 | 0 | ((transistor with (implantation implant$3)) and void) and ((implanting implantation implant$2) with (buble $5buble)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:26 |
| 49 | 5 | ((transistor with (implantation implant$3)) and void) and ((implanting implantation implant$2) with (cavit$3)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:26 |
| 48 | 91 | ((transistor with (implantation implant$3)) and void) and ((implanting implantation implant$2) with (void)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/05/12 14:27 |
| 51 | 1 | | USPAT | 2003/05/12 14:52 |
| 52 | 1 | | USPAT | 2003/05/12 14:53 |
| 53 | 1 | | USPAT | 2003/05/12 14:53 |

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L49: (5) 47 and ((implanting implantation implant$2) with (cavit$3))

L48: (91) 47 and ((implanting implantation implant$2) with (void))

L51: (1) "5953622".PN.

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| 1 | ☐ | ☐ | US 20020135041 A1 | 20020926 | 41 | Semiconductor integrated circuit and semiconductor device | 257/510 | 257/E27.085; 257/E29.134; |
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| 8 | ☐ | ☐ | US 20010008787 A1 | 20010719 | 16 | Method of forming complementary type conductive regions on a substrat | 438/258 | 438/264 |
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| 10 | ☐ | ☐ | US 20010001500 A1 | 20010524 | 22 | Semiconductor device and method for producing same | 257/506 | |
| 11 | ☐ | ☐ | US 6503799 B2 | 20030107 | 19 | Method of manufacturing semiconductor device | 438/269 | 438/341; 438/412; |
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L49: (5) 47 and ((implanting implantation implant$2) with (cavit$3))

L48: (91) 47 and ((implanting implantation implant$2) with (void))

L51: (1) "5953622".PN.

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| 13 | ☐ | ☐ | US 6461967 B2 | 20021008 | 86 | Material removal method for forming a structure | 438/705 | 216/38; 216/87; |
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| 15 | ☐ | ☐ | US 6350638 B1 | 20020226 | 16 | Method of forming complementary type conductive regions on a substrat | 438/199 | 257/E21.637; 257/E21.638; |
| 16 | ☐ | ☐ | US 6333217 B1 | 20011225 | 36 | Method of forming MOSFET with channel, extension and pocket implan | 438/197 | 257/E21.435; 257/E21.437; |
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| 19 | ☐ | ☐ | US 6281532 B1 | 20010828 | 13 | Technique to obtain increased channel mobilities in NMOS transisto | 257/288 | 257/418; 257/E21.195; |
| 20 | ☐ | ☐ | US 6281081 B1 | 20010828 | 7 | Method of preventing current leakage around a shallow trench isolation stru | 438/296 | 257/E21.546; 438/424; |
| 21 | ☐ | ☐ | US 6261964 B1 | 20010717 | 91 | Material removal method for forming a structure | 438/705 | 257/E21.011; 257/E21.166; |
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L49: (5) 47 and ((implanting implantation implant$2) with (cavit$3))

L48: (91) 47 and ((implanting implantation implant$2) with (void))

L51: (1) "5953622".PN.

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| 25 | ☐ | ☐ | US 6214700 B1 | 20010410 | 19 | Semiconductor device and method for producing same | 438/450 | 257/374; 257/E21.552; |
| 26 | ☐ | ☐ | US 6201278 B1 | 20010313 | 28 | Trench transistor with insulative spacers | 257/330 | 257/332; 257/336; |
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| 32 | ☐ | ☐ | US 6074902 A | 20000613 | 16 | Method of forming complementary type conductive regions on a substrat | 438/199 | 257/E21.637; 257/E21.638; |
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| 34 | ☐ | ☐ | US 6057194 A | 20000502 | 28 | Method of forming trench transistor in combination with trench array | 438/270 | 257/E21.428; 257/E21.429; |
| 35 | ☐ | ☐ | US 6054370 A | 20000425 | 11 | Method of delaminating a pre-fabricated transistor layer from a | 438/456 | 257/E21.568; 438/457; |
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L48: (91) 47 and ((implanting implantation implant$2) with (void))

L51: (1) "5953622".PN.

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| 37 | ☐ | ☐ | US 6025633 A | 20000215 | 8 | Multi-level transistor fabrication method having an inverted, upper leve | 257/369 | 257/343; 257/350; |
| 38 | ☐ | ☐ | US 6005272 A | 19991221 | 21 | Trench transistor with source contact in trench | 257/344 | 257/330; 257/332; |
| 39 | ☐ | ☐ | US 5986311 A | 19991116 | 21 | Semiconductor device having recrystallized source/drain regions | 257/382 | 257/347; 257/66; |
| 40 | ☐ | ☐ | US 5970331 A | 19991019 | 13 | Method of making a plug transistor | 438/199 | 257/274; 257/369; |
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| 46 | ☐ | ☐ | US 5888880 A | 19990330 | 19 | Trench transistor with localized source/drain regions implanted throug | 438/424 | 257/E21.429; 257/E29.267; |
| 47 | ☐ | ☐ | US 5882959 A | 19990316 | 9 | Multi-level transistor fabrication method having an inverted, upper leve | 438/152 | 257/E21.614; 257/E27.026; |
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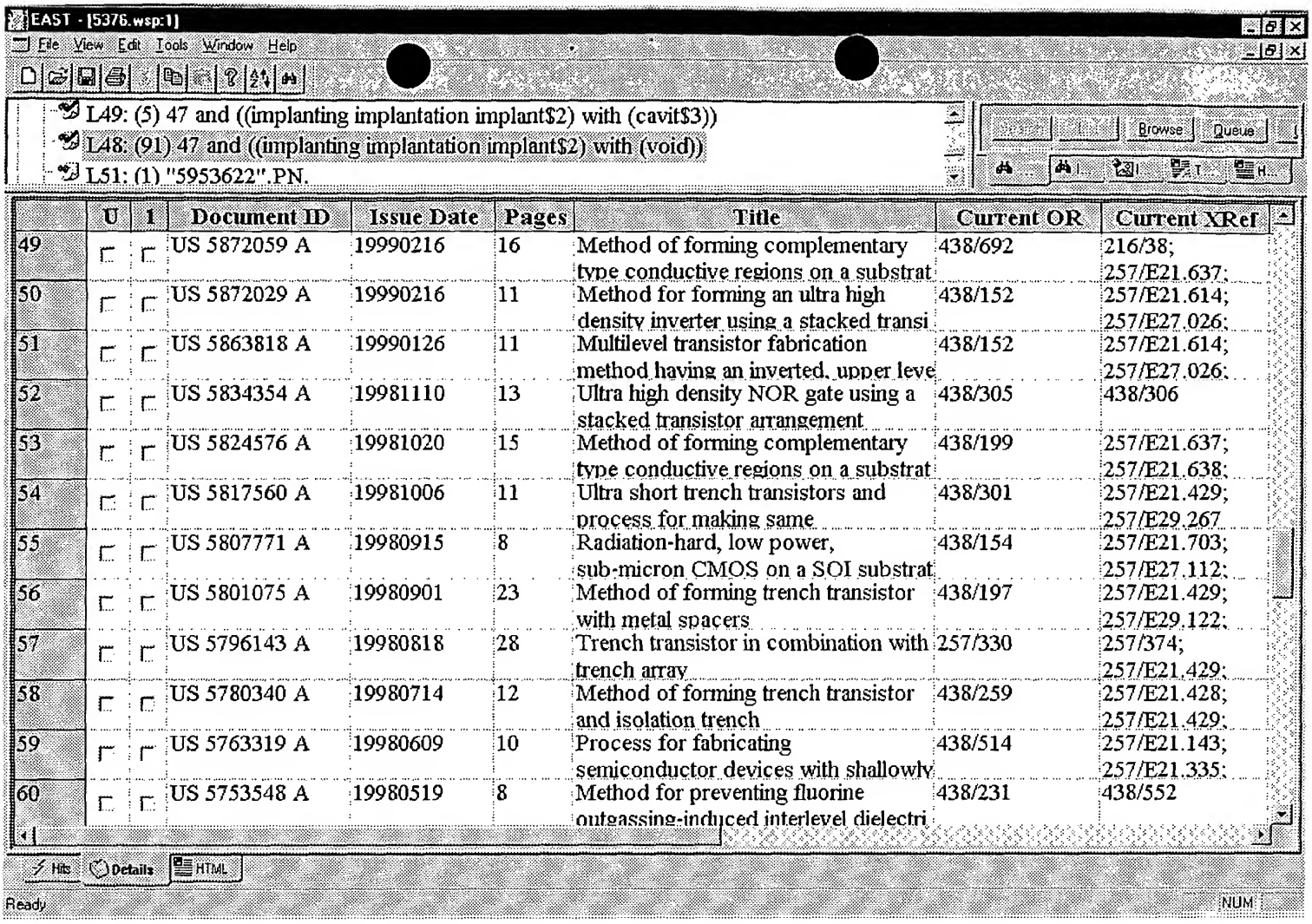


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| 49 | ☐ | ☐ | US 5872059 A | 19990216 | 16 | Method of forming complementary type conductive regions on a substrat | 438/692 | 216/38; 257/E21.637; |
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| 60 | ☐ | ☐ | US 5753548 A | 19980519 | 8 | Method for preventing fluorine outgassing-induced interlevel dielectri | 438/231 | 438/552 |

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L49: (5) 47 and ((implanting implantation implant$2) with (cavit$3))

L48: (91) 47 and ((implanting implantation implant$2) with (void))

L51: (1) "5953622".PN.

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| 83 | ☐ | ☐ | US 4398964 A | 19830816 | 6 | Method of forming ion implants self-aligned with a cut | 438/526 | 257/E21.024; 257/E21.346; |
| 84 | ☐ | ☐ | US 3841918 A | 19741015 | 11 | METHOD OF INTEGRATED CIRCUIT FABRICATION | 438/331 | 148/DIG.117; 148/DIG.85; |
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| 86 | ☐ | ☐ | US 6362082 B | 20020326 | 13 | Improvement of short channel effect in transistor involves implanting subst | | |
| 87 | ☑ | ☐ | US 6228694 B | 20010508 | | Carrier mobility modifying method for transistor involves forming channe | | |
| 88 | ☑ | ☐ | US 6191019 B | 20010220 | | Prevention of void formation in gate of transistor formed in substrate com | | |
| 89 | ☑ | ☐ | US 6188110 B | 20010213 | | Integrated circuit, e.g. metal oxide semiconductor devices, includes isola | | |
| 90 | ☑ | ☐ | US 5807771 A | 19980915 | | Radiation hard, low power, sub-micron CMOS devices - fabricat | | |
| 91 | ☑ | ☐ | US 5753548 A | 19980519 | | Forming N-channel and P-channel FETs, especially for CMOS circuits - | | |

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